REMARKS

Reconsideration and further examination of the application, as amended, are requested. All objections and rejections are respectfully traversed.

Request for Information

At p. 2, the Office Action requests information that could reasonably be used in a 102 or 103 rejection. Specifically, information regarding "an invalidate message that includes bits (masks) that indicate a path to processors". Applicants state that they have made a good faith attempt to obtain such information, but are not aware of any such information. Applicants are, however, submitting herewith an Information Disclosure Statement (IDS) pursuant to 37 CFR 1.97 for the Examiner's consideration.

§102 Rejection

Claims 1-17 were rejected under 35 U.S.C. §102 as being anticipated by the admitted prior art described by the Applicants in the Background Information section of their patent application.

Claim 1, as amended, in relevant part recites as follows:

> "A method of operating a cache coherency mechanism for a computer system that includes multiple processors, the method comprising"
>
> "determining paths through various switching devices on routes from an associated home node to the processors that have copies of the data of interest", and
>
> "encoding information that is indicative of the paths **into one or more masks**".

The prior art described in the Background section of the patent application fails, among other things, to disclose either (1) determining paths from a home node to the processors that have copies of the data of interest, or (2) or the encoding of information indicative of paths "into one or more masks".

The Office Action at pp. 4-5 contends that the intermediate switches of the multiprocessor computer system described at p. 3 of the Background Information section correspond to the recited "paths through various switching devices". The claim, however, recites "**determining paths** through various switching devices on routes from an associated home node to the processors that have copies of the data of interest". The Office Action fails to point to any part of the Background Information section of Applicants' patent application as purportedly disclosing the determination of paths. The Background, moreover, contains no disclosure of determining paths through switches on routes from a home node to those processors having copies of data of interest.

Next, the Office Action at p. 5 contends that the "presence bits" or "directory entries" described at p. 3 of the Background Information section of Applicants' patent application correspond to the recited "encoding information indicative of the paths into one or more masks". Applicants respectfully disagree. Neither the presence bits nor the directory entries provide information that is indicative of the paths from the home node to the processors having copies of the data of interest.

As the name implies and as specifically described at the top of p. 3, "presence bits" simply indicate at which processors within the multiprocessor system a copy of data associated with a given directory entry is currently "present". For example, if the multi-

processor system has 100 processors, the presence bits may indicate that processors 10, 22, 51 and 87 each have a copy of the data. The presence bits provide no information that is "indicative **of the paths**" from the home node to those processors. Instead, the presence bits merely indicate which of the processors within the multiprocessor system have a copy of the data of interest.

The directory entry itself also fails to disclose the recited "encoding information that is indicative of the paths **into one or more masks**". A directory entry simply specifies (1) a particular data item, (2) which processor (if any) is the owner of that data item, and (3) which processors (if any) have a copy of that data item (e.g., through the presence bits). Again, there is nothing in a directory entry that provides information "indicative of the paths" to those processors.

Because the Background Information section of Applicants' patent application fails to disclose either the determining of paths from a home node to processors having copies of a data item of interest, or the encoding of information indicative of the paths into one or more masks, the rejection of independent claims 1 and 6 should be withdrawn.

Independent claim 11 similarly recites, among other things, "one or more encoders for encoding into one or more masks information relating to paths through the switching devices from an associated home node to the processors that have data of interest". As set forth above, the Background Information section of Applicants' patent application fails to disclose such an encoder. Accordingly, the rejection of claim 11 should also be withdrawn.

At p. 5, the Office Action states that "the examiner believes all dependent claim features not specifically discussed above are expressly or inherently taught by the admitted prior art". Applicants respectfully disagree. Furthermore, as set forth in the MPEP, "in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." See MPEP §2112. Applicants respectfully submit that the Office Action fails to meet this standard. The Office Action provides no explanation at all to support its inherency rejection of the dependent claims. Accordingly, the rejection fails to satisfy the requirement of the MPEP, and therefore should be withdrawn.

In fact, the dependent claims are directed to further novel features of the present invention. For example, claim 4 recites that encoding includes setting bits that correspond to "ports of the respective switching devices". Claim 12 recites that the switching devices are organized into layers, and the masks relate "to paths through the switching devices in the associated layers". Accordingly, the dependent claims are also allowable.

Applicants have amended claims 1-9 and 11-17 to remove the "steps of" and other language, thereby broadening these claims. No new matter is being introduced. Applicants have also corrected several minor, typographical errors that were discovered in the Specification.

Applicants submit that the application, as amended, is in condition for allowance and early favorable action is respectfully requested.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Respectfully submitted,

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